FPGA Mezzanine Card
DSP Module

T. Janicki, R. Cieszewski
Agenda

1. Origin of this work
2. FMC standard
3. Idea(s) for DSP FMC
4. DSP and FPGA – short glance
5. Architecture
6. Done and To Do
1. Origin of this work

➢ JET – Joint European Torus Magnetic confinement plasma physics experiment

➢ Experiment produces ~300 Gb/s of data

➢ Major (only some) diagnostics:
  – Visible/infrared video cameras
  – Thomson scattering spectroscopy
  – Visible/UV/X-ray spectrometers

➢ Data mining system:
  – scalable via FPGA Mezzanine Card Standard
2. FMC Standard

- Mechanical
  - single width module card
  - connector (LPC, HPC)

- FMC common pinout
  - clocks
  - JTAG
  - I2C
  - power (12V, 3.3V, custom)

- LPC pinout
  - 34 pairs user-defined signals
  - one MGT pair

- HPC pinout
  - 80 pairs user-defined signals
  - 10 MGT pairs
  - additional clocks

69 x 76.5 mm
3. Idea(s) for DSP FMC

➢ To fit 2 DSP's on FMC
➢ To use fast interfaces – PCIe, SRIO
➢ HDMI with external adapter to use GbE
➢ To construct network connectivity utilizing various topologies
➢ To use FPGA – master to DSP's – coprocessor to DSP's
4. DSP and FPGA – short glance

- Texas Instruments – C6678
- Multi Core – up to 8 cores
- Interfaces – PCIe, SRIO, SGMII, DDR3
- Dedicated link – p2p HyperLink
- Up to 1.2 GHz
4. DSP and FPGA – short glance

➢ Xinlinx Spartan-6
  – XC6SLX45T

➢ Benefits
  – package 15x15 mm
  – 4xGTP transceivers
  – PCIe endpoint x1
  – 2 MCB's DDR3
  – 4 banks
  – 190 IO's
5. Architecture

- **SDMII**
- **USB and Conf Mem**
- **DDR3 Controller**
- **DP**
- **SRIO x1**
- **PCle x1 Gen2 Hyper Link**
- **3.125 Gb/s**
- **666 MHz**
- **FPGA**
- **PCle 2 x1 Gen1**
- **Hyper Link up to 50 Gb/s**
- **3.125 Gb/s**
- **1600 MHz**
- **HDMI**
- **Conf. MEM**
- **USB and Conf Mem**
- **FMC Connector**
- **I2C**
- **FMC EEPROM**
- **TEMP Sensor**
- **CLOCK Gen**
- **PDN**
- **Management**
6. Done and To Do

➢ Schematics probably complete
  – there was already 2 iterations changing the concept

➢ Programing FPGA
  – check'ed for early errors and tips

➢ Component placement on PCB (3'rd iteration)
  – focused to ease the routing of HF signals

➢ To do: routing PCB and programing DSP
  – use of Code Composer Studio (available)
  – devkit available in May/June
Thank you for listening

tomasz.janicki.tj@gmail.com

r.cieszewski@gmail.com

Questions please